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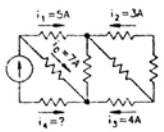
GATE - 1997

Electronics and Communication Engineering

1. For each of the followting questions (1.1—1.11), four alternatives *a*, *b*, *c* and *d* are given.

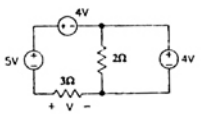
1.1 The current i_4 in the circuit of the figure is equal to



(*a*) 12A (*b*) – 12A

(*c*) 4A (*d*) None of these

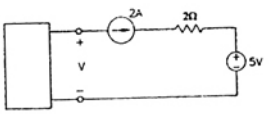
1.2 The voltage V in the figure is equal to



(*a*) 3V (*b*) – 3 V

(*c*) 5 V (*d*) None of these

1.3 The voltage V in the figure is always equal to



(*a*) 9 V (*b*) 5 V

(*c*) 1 V (*d*) None of the above

1.4 The function $f(t)$ has the Fourier Transform $g(\omega)$. The Fourier Transform

$$f f(t)\, g(t) \left(= \int_{-\infty}^{\infty} g(t)\, e^{-j\omega t}\, dt \right) \text{ is}$$

(*a*) $\frac{1}{2\pi} f(\omega)$ (*b*) $\frac{1}{2\pi} f(-\omega)$

(*c*) $2\pi f(-\omega)$ (*d*) None of the above

1.5 The Laplace Transform of $e^{\alpha t} \cos(\alpha t)$ is equal to

(*a*) $\frac{(s-\alpha)}{(s-\alpha)^2+\alpha^2}$ (*b*) $\frac{(s+\alpha)}{(s-\alpha)^2+\alpha^2}$

(*c*) $\frac{1}{(s-\alpha)^2}$ (*d*) None of the above

1.6 A transmission line of 50 Ω characteristic impedance is terminated with a 100 Ω resistance. The minimum impedance measured on the line is equal to

(*a*) 0 Ω (*b*) 25 Ω

(*c*) 50 Ω (*d*) 100 Ω

1.7 A rectangular air-filled waveguide has cross section of 4 cm × 10 cm. The minimum frequency which can propagate in the waveguide is

(*a*) 1.5 GHz (*b*) 2.0 GHz

(*c*) 2.5 GHz (*d*) 3.0 GHz

1.8 The line code that has zero dc component for pulse transmission of random binary data is

(*a*) Non-return to zero (NRZ)

(*b*) Retrun to zero (RZ)

(*c*) Alternate Mark Inversion (AM)

(*d*) None of the above

1.9 A probability density fucntion is given by

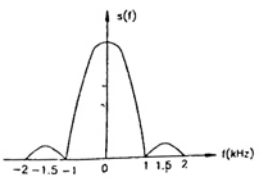
$p(x) = K e^{-x^2/2} \quad -\infty < x < \infty.$

The value of K should be

(*a*) $\frac{1}{\sqrt{2\pi}}$ (*b*) $\sqrt{\frac{2}{\pi}}$

(*c*) $\frac{1}{2\sqrt{\pi}}$ (*d*) $\frac{1}{\pi\sqrt{2}}$

1.10 A determininistic signal has the power spectrum given in the figure is, The minimum sampling rate needed to completely represent this signal is



(*a*) 1 *k*Hz (*b*) 2 *k*Hz

(*c*) 3 *k*Hz (*d*) None of the above

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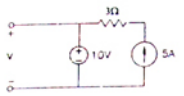
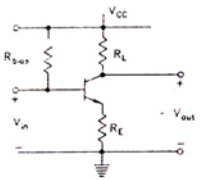
1.11 The voltage V in the figure is



(a) 10 V (b) 15 V
(c) 5 V (d) None of the above

2. For each of the following (2.1—2.10), alternatives *a*, *b*, *c* and *d* are given. Indicate the correct or the best answer by writing the letter *a*, *b*, *c* or *d* against the corresponding question number. All parts of this question must be attempted strictly in order. (10 × 1 = 10)

2.1 In the BJT amplifier shown in the figure is the transistor is based in the forward active region. Putting a capacitor across R_E will



(a) decrease the voltage gain and decrease the input impedance
(b) increase the voltage gain and decrease the input impedance
(c) decrease the voltage gain and increase the input impedance
(d) increase the voltage gain and increase the input impedance

2.2 A cascade amplifier stage is equivalent to
(a) a common emitter stage followed by a common base stage
(b) a common base stage followed by an emitter follower
(c) an emitter follower stage followed by a common base stage
(d) a common base stage followed by a common emitter stage

2.3 For a MOS capacitor fabricated on a *p*-type semiconductor, strong inversion occurs when
(a) surface potential is equal to Fermi potential
(b) surface potential is zero
(c) surface potential is negative and equal to Fermi potential in magnitude
(d) surface potential is positive and equal to twice the Fermi potential

2.4 In a common emitter BJT amplifier, the maximum usable supply voltage is limited by
(a) Avalanche breakdown of Base-Emitter junction
(b) Collector-Base breakdown voltage with emitter open (BV_{CBO})
(c) Collector-Emitter breakdown voltage with base open (BV_{CEO})
(d) Zener breakdown voltage of the Emitter-Base junction

2.5 Each cell of a static Random Access Memory contains
(a) 6 MOS transistors
(b) 4 MOS transistors and 2 capacitors
(c) 2 MOS transistors and 4 capacitors
(d) 1 MOS transistor and 1 capacitor

2.6 A 2 bit binary multiplier can be implemented using
(a) 2 inputs ANDs only
(b) 2 input XORs and 4 input AND gates only
(c) Two 2 inputs NORs and one XNOR gate
(d) XOR gates and shift registers

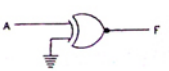
2.7 In standard TTL, the 'totem pole' stage refers to
(a) the multi-emitter input stage
(b) the phase splitter
(c) the output buffer
(d) open collector output stage

2.8 The inverter 74 ALSO4 has the following specifications

$I_{OHmax} = -0.4\ mA$, $I_{OLmax} = 8\ mA$, $I_{iHmax} = 20\ mA$, $I_{iLmax} = -0.1\ mA$,

The fan out based on the above will be
(a) 10 (b) 20
(c) 60 (d) 100

2.9 The output of the logic gate in the figure is



(a) 0
(b) 1
(c) A
(d) F

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2.10 In an 8085 μ P system, the RST instruction will cause an interrupt

(*a*) only if an interrupt service routine is not being executed

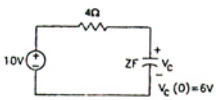
(*b*) only if a bit in the interrupt mask is made 0

(*c*) only if interrupts have been enabled by an EI instruction

(*d*) None of the above

3. For each of the following (3.1—3.11), four alternatives, *a*, *b*, *c* and *d* are given.

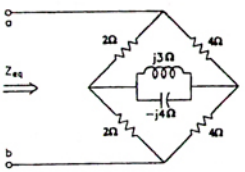
3.1 In the circuit of the figure is the energy absorbed by the 4 Ω resistor in the time interval $(0, \infty)$ is



(*a*) 36 Joules (*b*) 16 Joules

(*c*) 256 Joules (*d*) None of the above

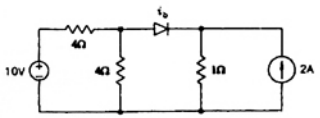
3.2 In the circuit of the figure is the equivalent impedance seen across terminals *a*, *b* is



(*a*) $\left(\frac{16}{3}\right)\Omega$ (*b*) $\left(\frac{8}{3}\right)\Omega$

(*c*) $\left(\frac{8}{3}+12j\right)\Omega$ (*d*) None of the above

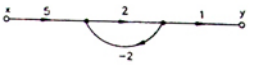
3.3 In the circuit of in the figure is the current i_D through the ideal diode (zero cut in voltage and forward resistance) equals



(*a*) 0 A (*b*) 4 A

(*c*) 1 A (*d*) None of the above

3.4 In the signal flow graph of the figure is y/x equals



(*a*) 3 (*b*) $\frac{5}{2}$

(*c*) 2 (*d*) None of the above

3.5 A certain linear time invariant system has the state and the output equations given below

$$\begin{bmatrix}\dot{X}_1\\ \dot{X}_2\end{bmatrix}=\begin{bmatrix}1 & -1\\ 0 & 1\end{bmatrix}\begin{bmatrix}X_1\\ X_2\end{bmatrix}+\begin{bmatrix}0\\ 1\end{bmatrix}u$$

$$y=[1\,1]\begin{bmatrix}X_1\\ X_2\end{bmatrix}$$

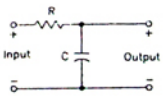
If $X_1(0)=1, X_2(0)=-1, u(0)=0$, then $\left.\frac{dy}{dt}\right|_{t=0}$ is

(*a*) 1 (*b*) −1

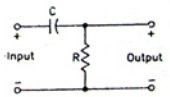
(*c*) 0 (*d*) None of the above

3.6 A communication channel has first order low pass transfer function. The channel is used to transmit pulses at a symbol rate greater than the half-power frequency of the low pass function. Which of the network shown in the figure is can be used to equalise the received pulses ?

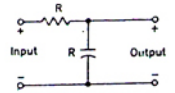
(*a*)



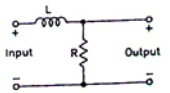
(*b*)



(*c*)



(*d*)



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3.7 The power spectral density of a deterministic signal is given by $[\sin(f)/f^2]$ where f is frequency. The autocorrelation function of this signal in the time domain is

(*a*) a rectangular pulse

(*b*) a delta function

(*c*) a sine pulse

(*d*) a triangular pulse

3.8 An amplifier A has 6 *d*B gain and 50 Ω input and output impedances. The noise figure of this amplifier as shown in the figure is (*a*) is 3 *d*B. A cascade of two such amplifiers as in the figure is will have a noise figure of

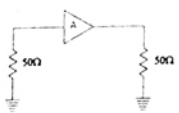


Fig. 3.8 (*a*)

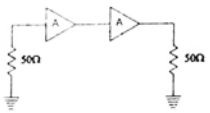


Fig. 3.8 (*a*)

(*a*) 6 *d*B (*b*) 8 *d*B

(*c*) 12 *d*B (*d*) None of the above

3.9 A parabolic dish antenna has a conical beam 2° wide, the directivity of the antenna is approximately

(*a*) 20 *d*B (*b*) 30 *d*B

(*c*) 40 *d*B (*d*) 50 *d*B

3.10 A very lossy, $\lambda/4$ long, 50 Ω transmission line is open circuited at the load end. The input impedance measured at the other end of the line is approximately

(*a*) 0 (*b*) 50 Ω

(*c*) ∞ (*d*) None of the above

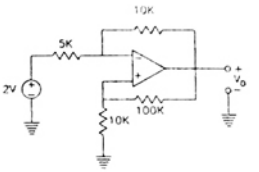
3.11 The skin depth at 10 MHz for a conductor is 1 cm. The phase velocity of an electromagnetic wave in the conductor at 1,000 MHz is about

(*a*) 6×10^6 m/sec (*b*) 6×10^7 m/sec

(*c*) 3×10^8 m/sec (*d*) 6×10^8 m/sec

4. For each of the following (4.1—4.10), four alternatives *a*, *b*, *c* and *d* are given.

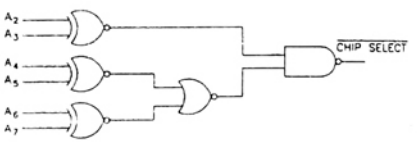
4.1 The output voltage V_0 of the circuit shown in the figure is



(*a*) −4 V (*b*) 6 V

(*c*) 5 V (*d*) −5.5 V

4.2 The decoding circuit shown in the figure is has been used to generate the active low chip select signal for a microprocessor peripheral. (The address lines are designated as AO to A7 for I/O addresses)



The peripheral will correspond to I/O addresses in the range

(*a*) 60 H to 63 H (*b*) A4 to A 7H

(*c*) 30 H to 33 H (*d*) 70 H to 73 H

4.3 The following insturctions have been executed by an 8085 μP

ADDRESS (HEX)	INSTRUCTION
6010	LXI H, 8A 79 H
6013	MOV A, L
6015	ADDH
6016	DAA
6017	MOV H, A
6018	PCHL

From which address will the next instruction be fetched ?

(*a*) 6019 (*b*) 6379

(*c*) 6979 (*d*) None of the above

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4.4 A signed integer has been stored in a byte using the 2's complement format. We wish to store the same integer in a 16 bit word. We should

(*a*) copy the original byte to the less significant byte of the word and fill the more significant with zeros

(*b*) copy the original byte to the more significant byte of the word and fill the less significant byte with zeros

(*c*) copy the original byte to the less significant byte of the word and make each fit of the more significant byte equal to the most significant bit of the original byte

(*d*) copy the original byte to the less significant byte as well as the more significant byte of the word

4.5 A half wave rectifier uses a diode with a forward resistance Rf. The voltage is $V_m \sin \omega t$ and the load resistance is R_L. The DC current is given by

(*a*) $\frac{V_m}{\sqrt{2}\, R_L}$ (*b*) $\frac{V_m}{\pi (R_f + R_L)}$

(*c*) $\frac{2Vm}{\sqrt{\pi}}$ (*d*) $\frac{V_m}{R_L}$

4.6 The intrinsic carrier density at 300 K is $1.5 \times 10^{10}/cm^3$, in silicon. For n-type silicon doped to 2.25×10^{15} atoms/cm^3, the equilibrium electron and hole densities are

(*a*) $n = 1.5 \times 10^{15}/cm^3$, $p = 1.5 \times 10^{10}/cm^3$

(*b*) $n = 1.5 \times 10^{10}/cm^3$, $p = 2.25 \times 10^{15}/cm^3$

(*c*) $n = 2.25 \times 10^{15}/cm^3$, $p = 1.0 \times 10^{5}/cm^3$

(*d*) $n = 1.5 \times 10^{10}/cm^3$, $p = 1.5 \times 10^{10}/cm^3$

4.7 For the NMOS logic gate shown in the figure is the logic function implemented is

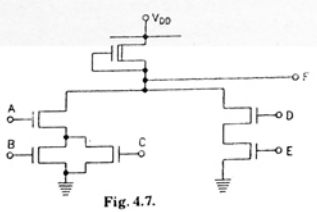
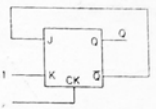


Fig. 4.7.

(*a*) $\overline{ABCDE}$ (*b*) $(AB + \overline{C}).\overline{(D + E)}$

(*c*) $\overline{A.(B + C) + D.E}$ (*d*) $\overline{(A + B)}.C + \overline{D}.\overline{E}$

4.8 In a J – K flip-flip we have J = Q and K = 1. Assuming the flip flop was initially cleared and then clocked for 6 puleses, the sequence at the Q output will be



(*a*) 010000

(*b*) 011001

(*c*) 010010

(*d*) 010101

4.9 The gate delay of an NMOS inverter is dominated by charge time rather than discharge time because

(*a*) the driver transistor has larger threshold voltage than the load transistor

(*b*) the driver transistor has larger leakage currents compared to the load transistor

(*c*) the load transistor has a smaller W/L ratio compared to the driver transistor

(*d*) none of the above

4.10 The boolean function A + BC is a reduced form of

(*a*) AB + BC (*b*) (A + B) . (A + C)

(*c*) $\overline{A}B + A\overline{B}C$ (*d*) (A + C) . B

5. In the following questions (5.1—5.6), match each of the items 1, 2 on the left with the most appropriate item *a*, *b*, *c* or *d* on the right. [e.g. If you feel 1 matches with *b* and 2 with *c*, write (1, *b*) (2, *c*)] (6 × 2 = 12)

5.1 In the case of a linear time invariant system

(1) Poles in the right half plane implies

(*a*) Exponential decay of output

(2) Impulse response zero for $t \le 0$ implies

(*b*) System is casual

(*c*) No stored energy in the system

(*d*) System is unstable.

5.2 If the Fourier Transform of deterministic signal g(t) is G(*f*), then

(1) The Fourier Transform of $g(t-2)$ is

(*a*) $G(f)e^{-j(4\pi f)}$

(2) The Fourier Transform of $g(t/2)$ is

(*b*) G (2*f*)

(*c*) 2G (2*f*)

(*d*) G (*f* – 2)

5.3 (1) An 8-bit wide 5 word sequential memory will have

(*a*) 8 Fixed 'AND' gates and 4 programmable 'OR' gates

(2) A 256 × 4 EFROM has

(*b*) Eight 4 bit shift registers

(*c*) 4 words of 32 bits each

(*d*) 8 address pins and 4 data pins output

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5.4 (1) Wave tilt

(*a*) Under-water propagation

(2) Faraday Rotation

(*b*) Ground wave propagation

(*c*) Space wave propagation

(*d*) Ionospheric propagation

5.5 While moving data between registers of the 8085 and the stack

(1) a PUSH instruction

(*a*) Pre increments the stack pointer

(2) a POP instruction

(*b*) Post increments the stack pointer

(*c*) Pre decrements the stack pointer

(*d*) Post decrements the stack pointer

5.6 Negative feedback in

(1) Voltage series configuration

(*a*) increase input impedance

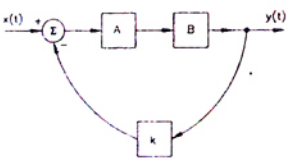
(2) Current shunt configuration

(*b*) decrease input impedance

(*c*) increases closed loop gain

(*d*) leads to oscillation

6.



The figure is shows the block diagram representation of control system. The system in block A has an impulse response $h_A(t) = e^{-t}\,u(t)$. The system in block B has an impulse response $h_B(t) = e^{-2t}\,u(t)$. The block 'K' amplifies its inputs by a factor k. For the overall system with input $x(t)$ and output $y(t)$ (5)

(*a*) Find the transfer function $\frac{Y(s)}{X(s)}$ when $k = 1$

(*b*) Find the impulse response when $k = 0$

(*c*) Find the values of k for which the system becomes unstable

Note: $u(t) = 0\ t \le 9$

$= 1\ t > 0$

7. Circuit shown in the figure is an NMOS shift register. All transistors are NMOS enhancement type with threshold voltage $V_T = 1V$. Supply used is $V_{DD} = 5V$ (5)

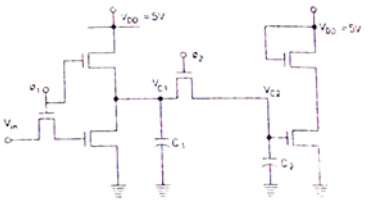


Fig. 7(a).

Two non-overlapping clocks ϕ_1 and ϕ_2 are as shown in the figure is and have large pulse widths.

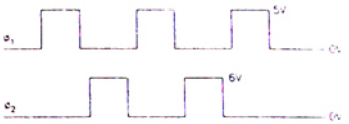
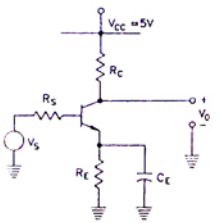


Fig. 7(b).

All capacitors are initially discharged and the input $Vin = 0$ volts is applied. If values of capacitors are $C_1 = 2\ pf$ and $C_2 = 1\ pf$, find out voltage V_{C2} on capacitor C_2 after ϕ_2 goes low. Neglect body-effect on V_T in your evaluation.

8. The transistor in the circuit shown in the figure is so biased (dc biasing network is not shown) that the dc collecter current $I_c = 1$ mA. Supply is $V_{cc} = 5V$. (5)



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$R_c = 2\ k\Omega$,

$R_s = 1.4\ k\Omega$

and $R_E = 100\ \Omega$

The transistor has specifications.

$\beta = 100$ and base spreading resistance

$r_{bb} = 100\ \Omega$.

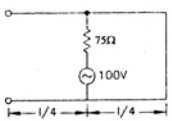
Assume $\frac{kT}{q} = 25$ mV.

Evaluate small signal Voltage Gain A_{V_s} at a frequency of 10 *k*Hz, and Input Resistance R_i for two cases

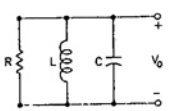
(*a*) CE, the hypass capacitor across R_E is 25 μF.

(*b*) The bypass capacitor C_E is removed leaving R_E unbypassed

9. $A\frac{\lambda}{2}$ section of a 600 Ω transmission line, short circuited at one end and open circuited at the other end, is shown in the figure is 100 V/75 Ω generator is connected at the mid point of the section as shown in the figure. Find voltage at the open circuited end of the line. **(5)**

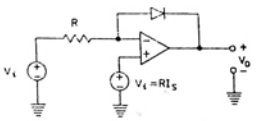


10. In the ciruit of the figure is
R = 100 Ω, L = 20 *n*H and C = 32 pF.
The circuit is maintained at a temperature of 300 K. Derive and plot the power spectral density of the voltage V_o. Mark all the relevant points on the plot with numerical values. (The Boltzmann constant $k = 1.28 \times 10{-}23$ J/K



Attempt any TEN questions from this section. (Each question carries 5 marks.)

11. Consider the circuit given in the figure is using an ideal operational amplifier.



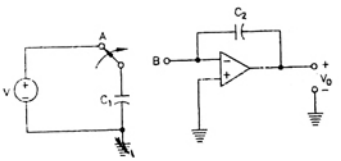
The characteristics of the diode are given by the relation $I = I_S\left(e^{\frac{V}{kT}} - 1\right)$

where V is the forward voltage across the diode.

(*a*) Express V_o as function of V_i assuming $V_i > 0$

(*b*) If $R = 100\ k\Omega$, $I_s = 1\ \mu A$ and $\frac{kT}{q} = 25\ m$V, find the input voltage V_i for which $V_o = 0$.

12. In the circuit shown in the figure is assume that the operational amplifier is ideal and that $V_o = 0$V initially. The switch is connected first to 'A' charging C_1 to the voltage V. It is then connected to the point 'B'. This process is repeated *f* times per second.



(*a*) Calculate the charge transferred per second from node A to node B.

(*b*) Derive the average rate of change of the output voltage V_o.

(*c*) If the capacitor and the switch are removed and a resistor is connected between points A and B, find the value of the resistor to get the same average rate of change of the output voltage ?

(*d*) If the repetition rate of the switching action is 10^4 times per second, $C_1 = 100$ *p*F, $C_2 = 10$ *p*F and V= 10 *m*V, what is the average rate of change of the output voltage ?

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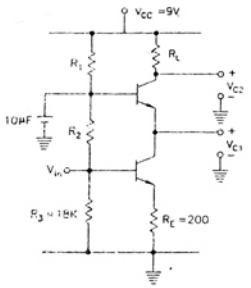
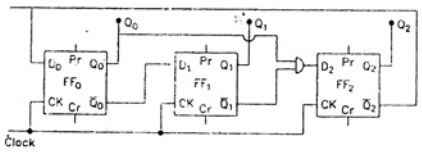


In the cascade amplifier circuit shown in the figure is determine the values of R_1, R_2 and R_L such that the quiescent current through the transistors is 1 mA and the collector voltages are $V_C = 3$ V and $V_{C2} = 6$ V, Take $V_{BE} = 0.7$ V, transistor β to be high and base currents to be negligible.

14. A sequence generator is shown in the figure is The counter status (Q_0, Q_1, Q_2) is initialised to 010 using preset/clear inputs.



The clock has a period of 50 ns and transitions take place at the rising clock edge.

(*a*) Give the sequence generate at Q_0 till it repeats.

(*b*) What is the repetition rate of the generated sequence ?

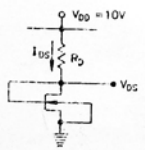
15. Given an NMOS circuit as shown in the figure is The specifications of the circuit are

$V_{DD} = 10$ V; $\beta = K = \mu_n C_{ox} (W/L) = 10^{-4}$ Amp/V^2

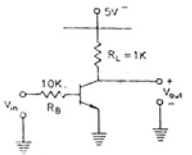
$V_T = 1$ V and $I_{DS} = 0.5$ *m*A.

Evaluate V_{DS} and R_D for the circuit.

Neglect body – effect for V_T.



shown in the figure is Transistor used is an *n-p-n* type with specifications as follows



$\beta_F = 70$

$V_{BEON} = 0.7$ V

$V_{BESAT} = 0.8$ V

$V_{CESAT} = 0.1$ V.

Also $R_L = 1\ k\Omega$;

$R_B = 10\ k\Omega$ and

supply $V_{CC} = 5$V.

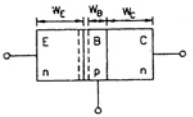
17. For a typical *n-p-n* transistor, as shown in the figure we have the following data available

(*a*) $W_C = 20\ \mu$m and Collcetor doping = 5×10^{18}/cc

(*b*) $W_E = 1\ \mu$m and Emitter doping = 10^{19}/cc

(*c*) Base doping = 5×10^{15}/cc

(*d*) Minority carrier life time in the Base region is $\tau_n = 5\ \mu$sec.



Under Punch-through condition the

$V_{BC} = 10\text{ V} + V_{bi}$ volts.

Here V_{bi} is the built in potential of Base-collector junction. Emitter Injection efficiency can be assumed as 1 for this transistor.

Evaluate Base Width W_B and the current gain α.

[Standard data for this question is : $q = 1.6 \times 10^{-19}$ coloumbs; $\frac{KT}{q} = 25\ mV$.

For silicon at T = 300 K, $D_n = 30$ cm^2/sec; $K_S \epsilon_o = 10^{-12}$ F/cm; $n_i = 1.5 \times 10^{10}$/cc]

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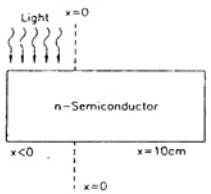
18. An n-type silicon bar is doped uniformly by phosphorous atoms to a concentration 4.5×10^{13}/cc. The bar has cross-section of 1 mm^2 and length of 10 cm. It is illuminated uniformly for region $x < 0$ as shown in the figure is. Assume optical generation rate 10^{21} Electron-Hole pairs per cm^3 per second, for this case. The hole lifetime and electron lifetime are equal, and equal to 1 μsec.

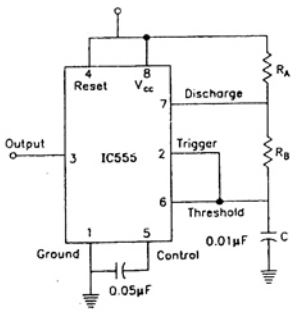


Evaluate the hole and electron diffusion currents at $x = 34.6$ μm.
Following expressions and data can be used in this evaluation

$$J_p = qD_p \frac{dp}{dx};\ Jn = qD_n \frac{dn}{dx}$$

where $D_p = 12\ cm^2/sec$; $d_n 30 = cm^2/sec$.
$q = 1.6 \times 10^{-19}$ coloumbs; $(kt/q) = 26\ mV$.

19. An IC 555 chip has been used to construct a pulse-Generator. Typical pin connections with components is shown below in the figure is for such an application. However it is desired to generate a square pulse of 10 kHz.



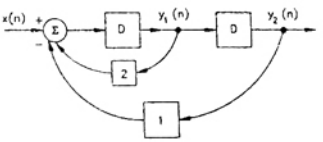
Evaluate values of R_A and R_B if the capacitor C has the value of 0.01 μF for the configuration chosen. If necessary you can suggest modification in the external circuit configuration.

20. An 8085 μP uses a 2 MHz crystal. Find the time taken by it to execute the following delay subroutine, inclusive of the call instruction in the calling program.

```
Calling program   DELAY:      PUSH PSW
... .....                     MVI A, 64 H
CALL              DELAY LOOP: NOP
.....                         DCR A
.....                         JNZ LOOP
                              POP PSW
                              RET
```

You are given that a CALL instruction takes 18 cycles of the system clock, PUSH requires 12 cycles and a conditional jump takes 10 cycles if the jump is taken and 7 cycles if it is not. All other instructions used above take $(3n + 1)$ clock cycles, where n is the number of accesses to the memory, inclusive of the opcode fetch.

21.



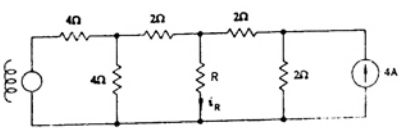
In the figure is a linear time invariant discrete systme is shown. Blocks labelled D represent unit delay elements. For $n < 0$, you may assume that $x(n), y_1(n), y_2(n)$ are all zero.

(a) Find the expression for $y_1(n)$ and $y_2(n)$ in terms of $x(n)$

(b) Find the transfer function $\frac{Y_2(z)}{X(z)}$ in the z - domain

(c) If $x(n) = 1$ at $n = 0$
$= 0$ otherwise,
find $y_2(n)$

22.



In the circuit of figure when R = 0 Ω, the current i_R equals 10A

(a) Find the value of R for which it absorbs maximum power

(b) Find the value of ε

(c) Find V_2 when $R = \infty$ (open circuit)

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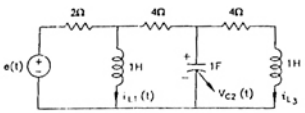
23.

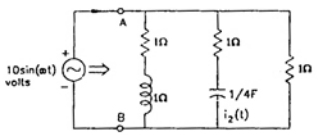


In the circuit of the figure is all currents and voltages are sinusoids of frequency ω rad/sec.

(*a*) Find the impedance to the right of (A, B) at $\omega = 0$ rad/sec and $\omega = \infty$ rad/sec.

(*b*) If $\omega = \omega_0$ rad/sec and $i_1(t) = I \sin(\omega_0 t)$ A, where I is positive $\omega_0 \neq 0$, $\omega_0 \neq \infty$ then find I, ω_0 and $i_2(t)$

24.



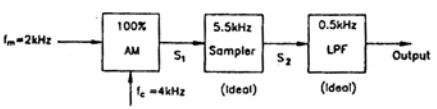
For the circuit shown in the figure is choose state variables X_1, X_2, X_3, to be $i_{L1}(t), V_{c2}(t), i_{L3}(t)$

(*a*) Write the state equations

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \end{bmatrix} = A \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} + B[e(t)]$$

(*b*) If $e(t) = 0, t \geq 0, i_{L1}(0) = 0, V_{C2}(0) = 0, i_{L3}(0) = 1$A, then what would the total energy dissipated in the resistors in the interval $(0, \infty)$ be?

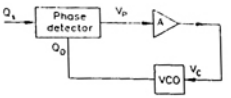
25. A block diagram of a system is shown in the figure is draw the spectrum of the output signal with relative aptitudes of the frequencies.



26. Find the mean of a function $X(T) = \sin^2(\alpha T)$, where α is a constant, and T is a random variable. The *pdf* of T is given by,

$$f(T) = e^{-T} \text{ for } T \geq 0$$
$$= 0 \text{ for } T < 0$$

27. The figure is shows the block diagram of phase-locked-loop (PLL) in the locked condition.



The output voltage of the phase detector is given by

$$V_p = K_d(\phi_i - \phi_0),$$

where ϕ_i = phase of the input signal, and

ϕ_0 = the phase of the output Voltage Controlled Oscillator (VOC).

The value of K_d is 1 Volt/radian,

The frequency deviation of the VCO output is,

$$\Delta f_0 = K_f V_C$$

where V_C = input voltage of the VCO, and

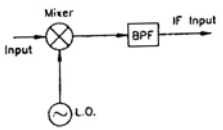
k_f = 159.15 Hz/volt.

The amplifier A is a buffer with a voltage gain of unity.

(*a*) Derive the transfer function $\phi_0(s)/\phi_i(s)$.

(*b*) Let the loop to be locked for time $t < 0$ and $\Phi_i(t) = u(t)$ radian, where $u(t)$ is the unit step function. Determine $\Phi_0(t)$ for $t > 0$.

28. The figure is shows the first stage of a superheterodyne receiver. The desired input signal is at a frequency of 700 MHz. The local oscillator (L.O) frequency is 1 GHz. The mixer is an ideal multiplier with a gain independent of frequency. A band-pass filter (BPF) is used to select the Intermediate Frequency (IF) output at 300 MHz.



(*a*) What is the image frequency of the desired input?

(*b*) A Low Pass Filter (LPF) can be used before the mixer to reject the image frequency. If a perfect rejection (zero transmission) of the image is desired, what type of LPF should be employed?

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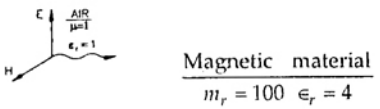
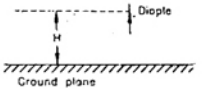
(c) The input in the figure is corrupted by an undesired 750 MHz signal which has the same amplitude as that of the desired signal at 700 MHz. Let the BPF be of second order. At the BPF output, the undesired signal should be 20 dB below the desired signal. Calculate the Q required for the BPF.

29. A uniform plane wave is normally incident from air on an infinitely thick magnetic material with relative permeability 100 and relative permittivity 4 see the figure is. The wave has an electric field of 1V, meter (rms). Find the average pointing vector inside the material.



30. A dipole antenna has a sin θ radiation pattern where the angle θ is measured from the axis of the dipole. The dipole is vertically located above an ideal ground plane the figure is. What should be the height of the dipole H in terms of wavelength so as to get a null in the radiation pattern at an angle of 45° from the ground plane ? Find the direction of maximum radiation also.



ANSWERS

1.1 (b)	1.2 (a)	1.3 (d)	1.4 (c)	1.5 (a)	1.6 (a)	1.7 (a)	1.8 (c)
1.9 (a)	1.10 (c)	1.11 (a)	2.1 (b)	2.2 (a)	2.3 (d)	2.4 (c)	2.5 (a)
2.6 (b)	2.7 (c)	2.8 (b)	2.9 (c)	2.10 (c)	3.1 (d)	3.2 (b)	3.3 (c)
3.4 (c)	3.5 (c)	3.6 (b)	3.7 (d)	3.8 (a)	3.9 (b)	3.10 (a)	3.11 (a)
4.1 (d)	4.2 (a)	4.3 (b)	4.4 (c)	4.5 (b)	4.6 (c)	4.7 (c)	4.8 (d)
4.9 (c)	4.10 (b)						

5.1 (1) – d, (2) – b **5.2** (1) – a, (2) – c

5.3 (1) – b, (2) – d **5.4** (1) – b, (2) – c

5.5 (1) – c, (2) – d **5.6** (1) – a, (2) – $\dot{b}$